

*Sub P
cont'd*

4 providing a second plurality of memory banks of semiconductor memory devices, each
5 memory bank being accessible to the first and second processors for operations selected from
6 the group comprising read and write operations; and

7 storing subsets of said audio data in the second plurality of memory banks, the subsets
8 corresponding to different groups of audio channels.

Sub Jd

1 3. (Amended) The method of claim 1 wherein [P is equal to two] the second
2 plurality of memory banks includes two memory banks.

Sub Jd

1 5. (Twice Amended) A system having first and second buses for processing real-
2 time audio data from a first plurality of audio channels, the system comprising:
3 a first processor and a second processor coupled to said first and second busses,
4 respectively; and

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5 a second plurality of memory banks of semiconductor memory devices coupled to said
6 first and second buses for storing said audio data, said second plurality of memory banks being
7 accessible to the first and second processors for operations selected from the group comprising
8 read and write operations, said second plurality of memory banks storing subsets of audio data,
9 said subsets corresponding to different groups of audio channels.

Sub Jd

1 6. (Amended) The system of claim 5 further comprises [P] a plurality of selectors
2 coupled said first and second buses to select said memory banks for access by one of said first
3 and second processors.

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7. (Amended) The system of claim 6 wherein [P] the plurality of selectors include
[P] a plurality of address multiplexers and [P] data transceivers.

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(Amended) The system of claims 5, wherein the [P] memory banks include
dynamic random access memories.

